FIG. 1(Prior Art)

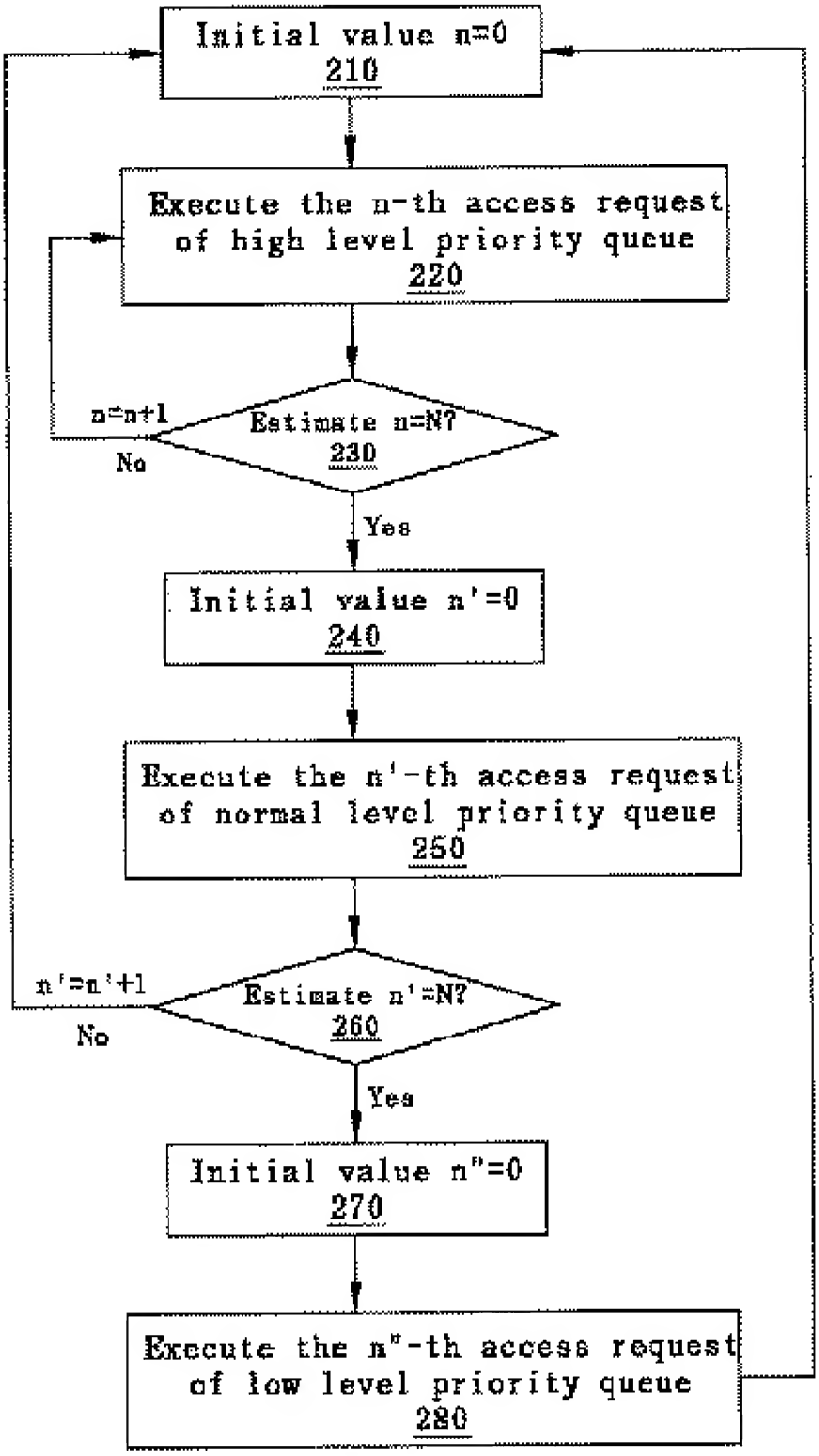

Initial value n=0
210
Execute the n-th access request of high level priority queue
220
n=n+1
Estimate n=N?
230
No
Yes
Initial value n'=0
240
Execute the n'-th access request of normal level priority queue
250
n'=n'+1
Estimate n'=N?
260
No
Yes
Initial value n"=0
270
Execute the n"-th access request of low level priority queue
280

FIG. 2

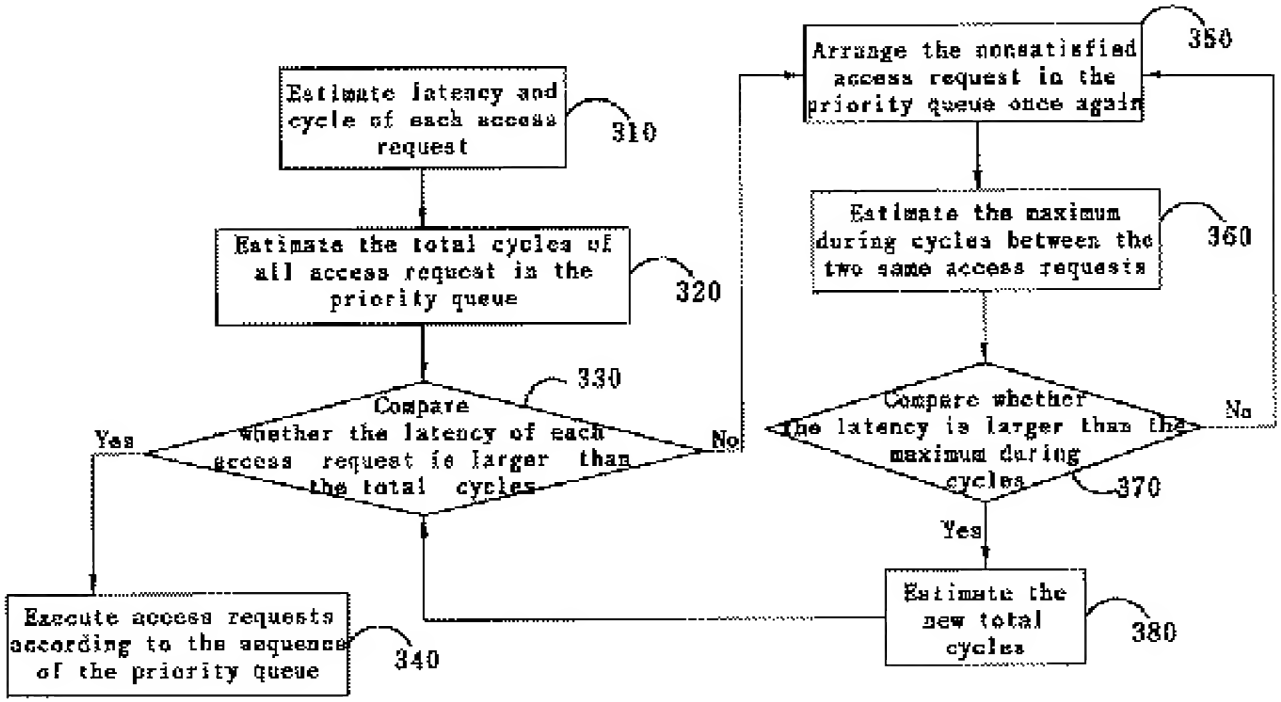

Estimate latency and cycle of each access request
310
Estimate the total cycles of all access request in the priority queue
320
330
Compare whether the latency of each access request is larger than the total cycles
Yes
No
Execute access requests according to the sequence of the priority queue
340
Arrange the nonsatisfied access request in the priority queue once again
350
Estimate the maximum during cycles between the two same access requests
360
Compare whether the latency is larger than the maximum during cycles
370
No
Yes
Estimate the new total cycles
380

FIG. 3

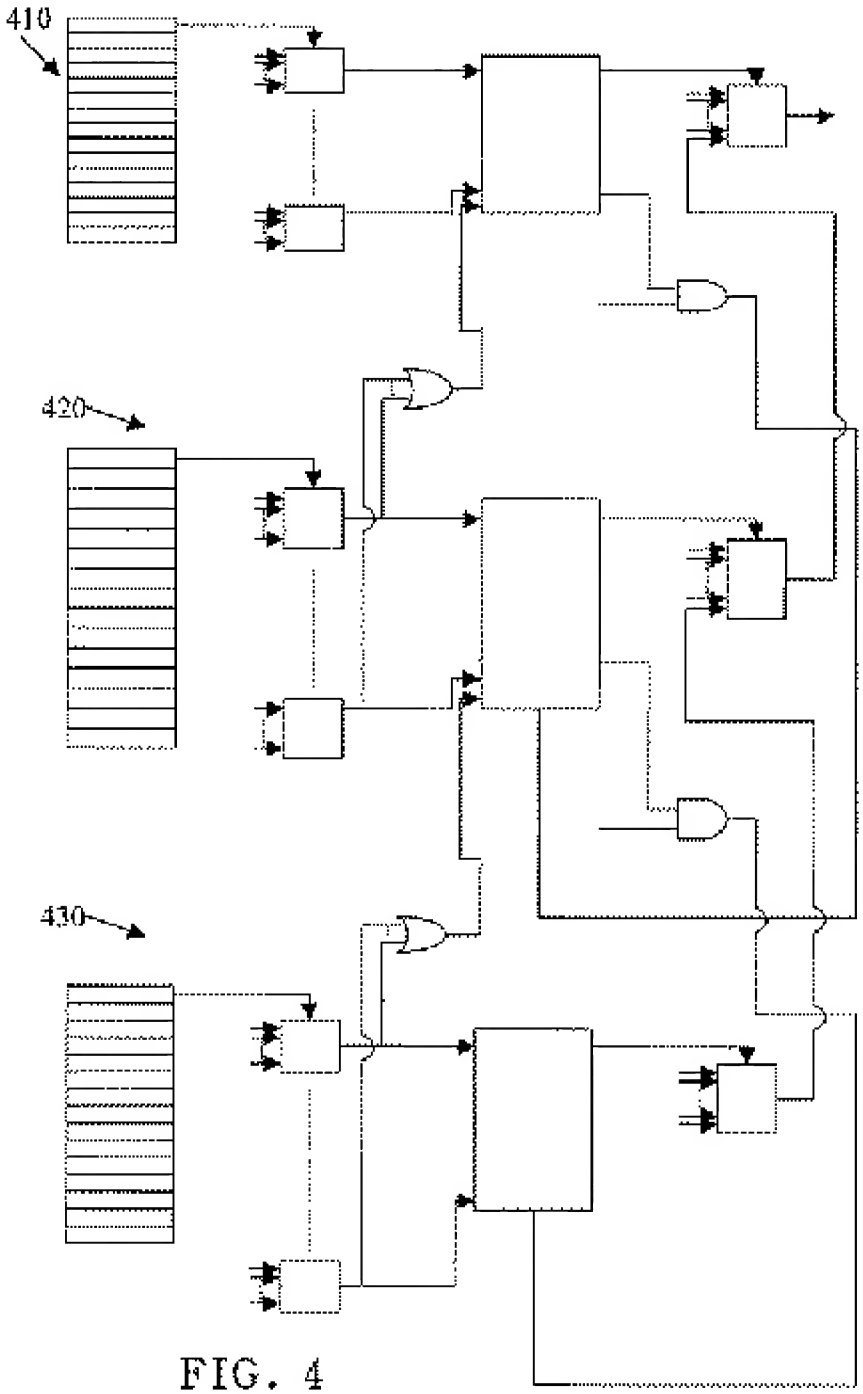


FIG. 4

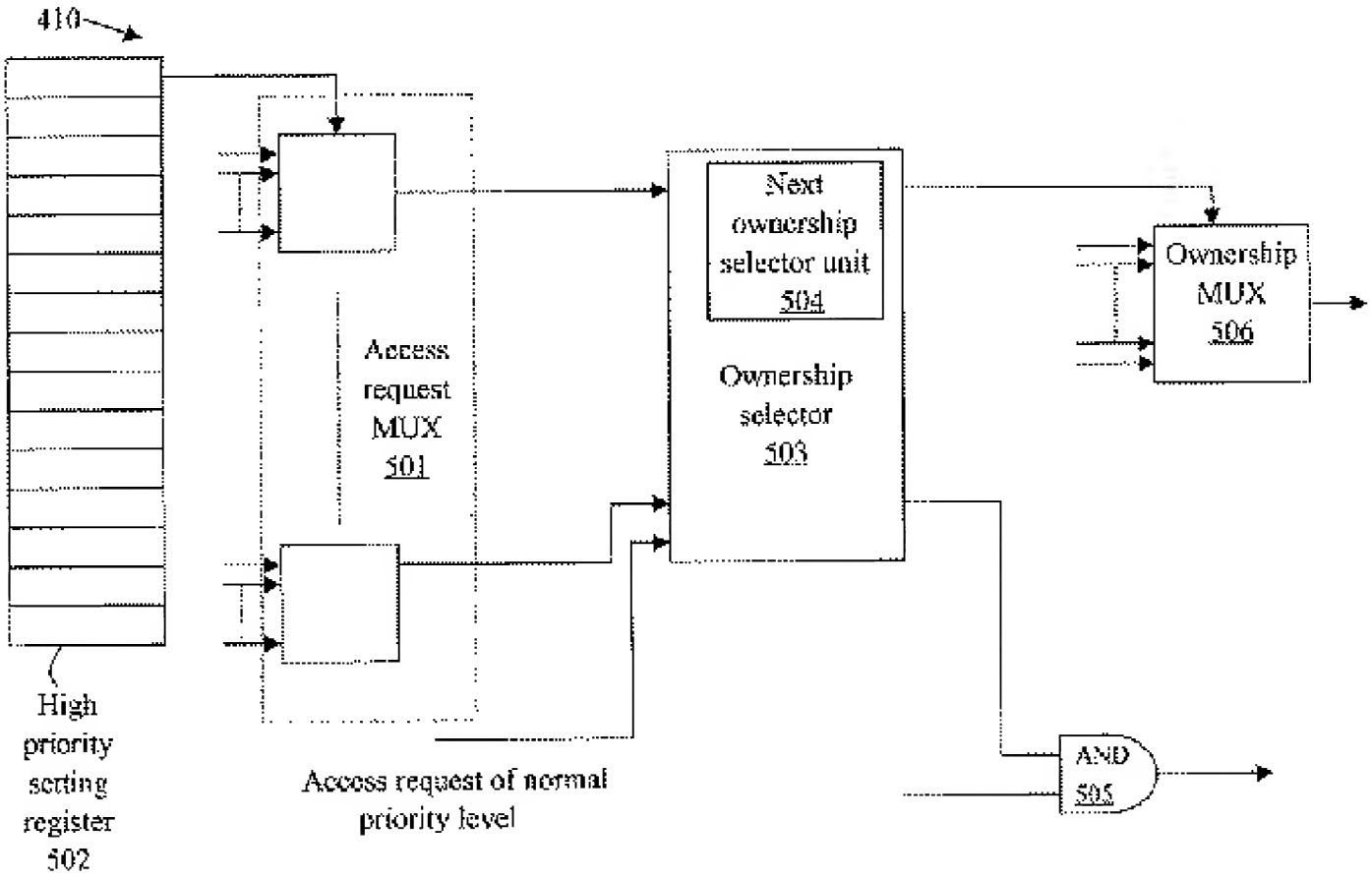

410
Access request MUX 501
Next ownership selector unit 504
Ownership selector 503
Ownership MUX 506
AND 505
High priority setting register 502
Access request of normal priority level

FIG. 5

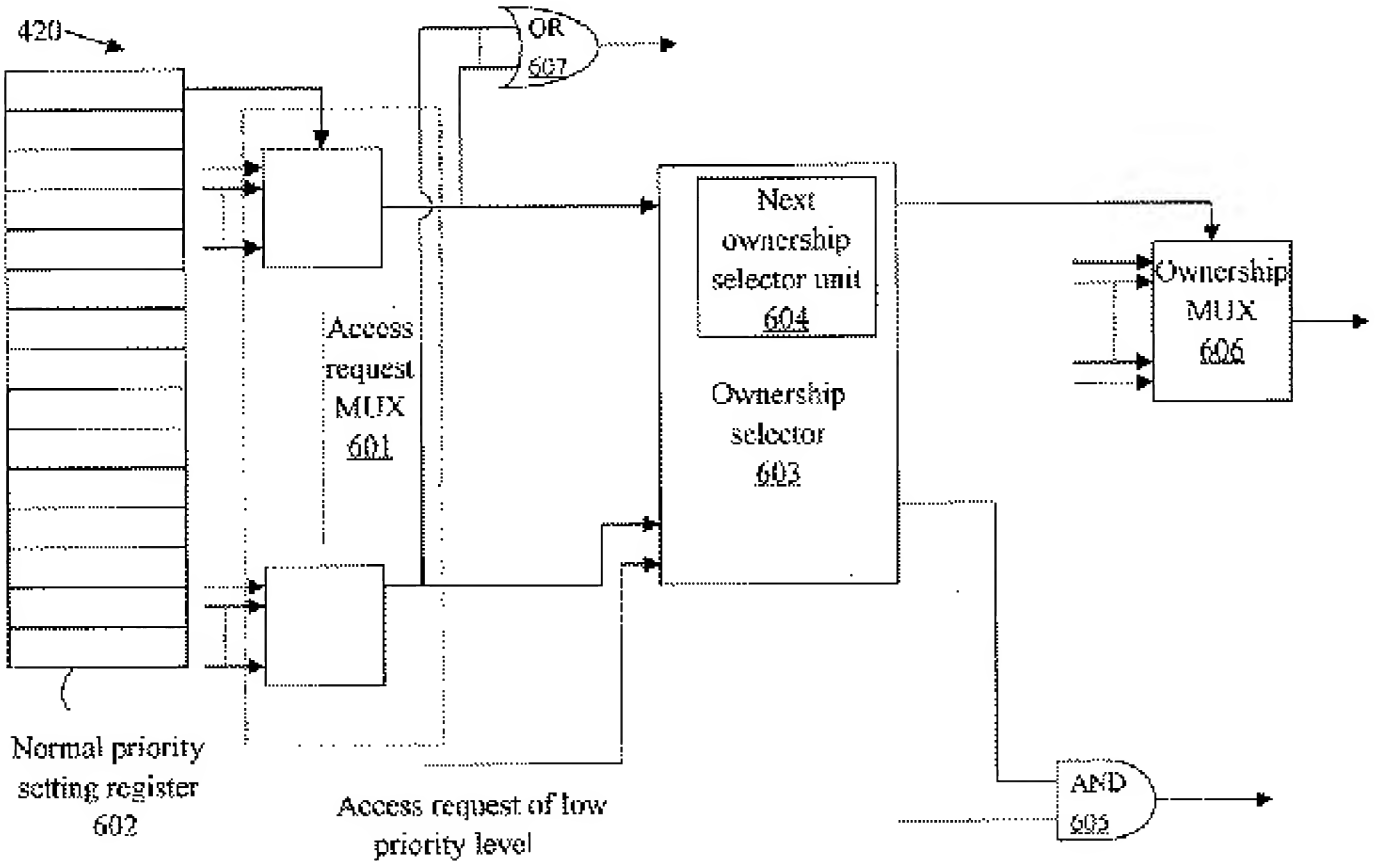

420
OR
607
Next
ownership
selector unit
604
Ownership
MUX
606
Access
request
MUX
601
Ownership
selector
603
Normal priority
setting register
602
Access request of low
priority level
AND
605

FIG. 6

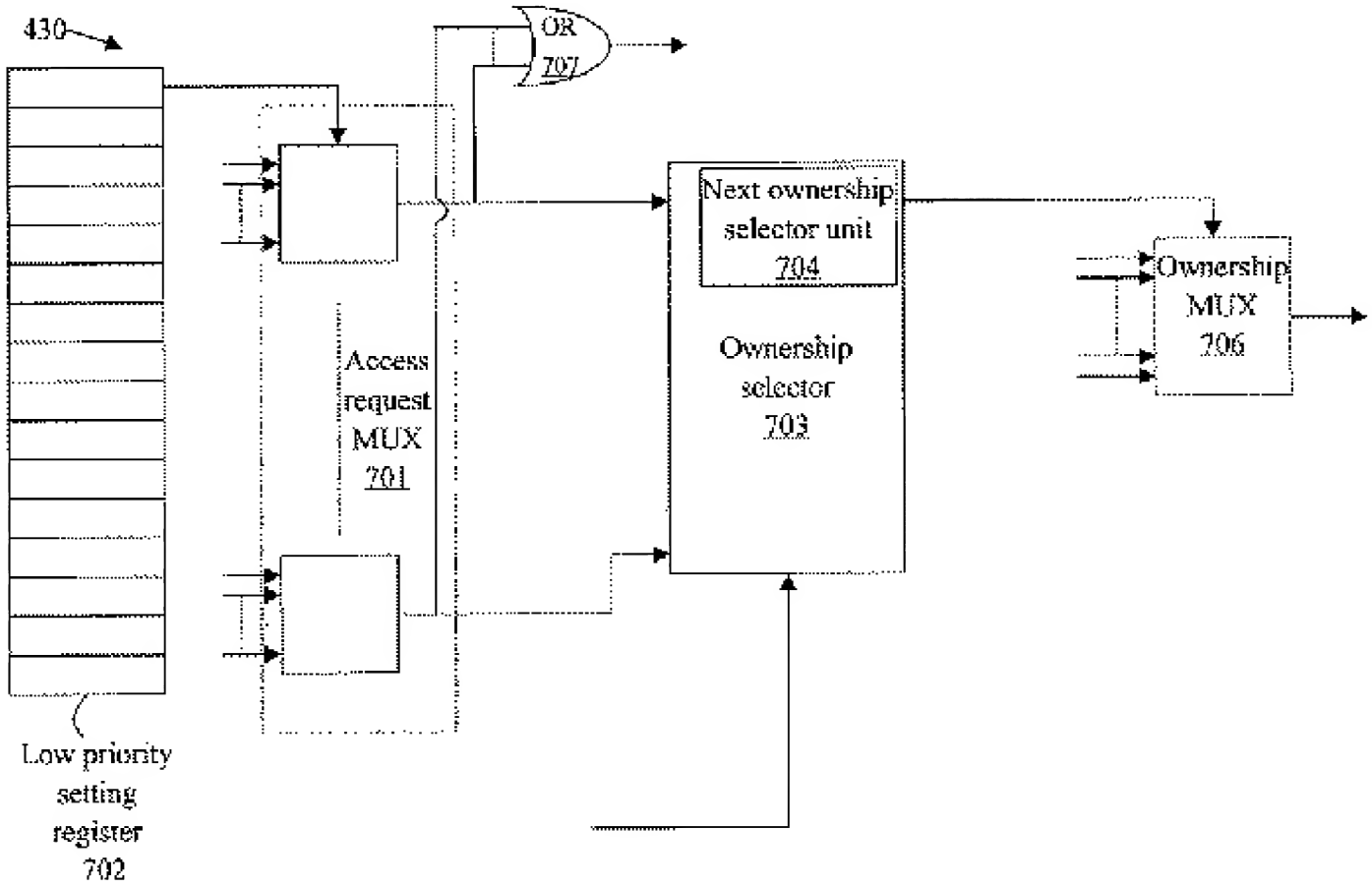
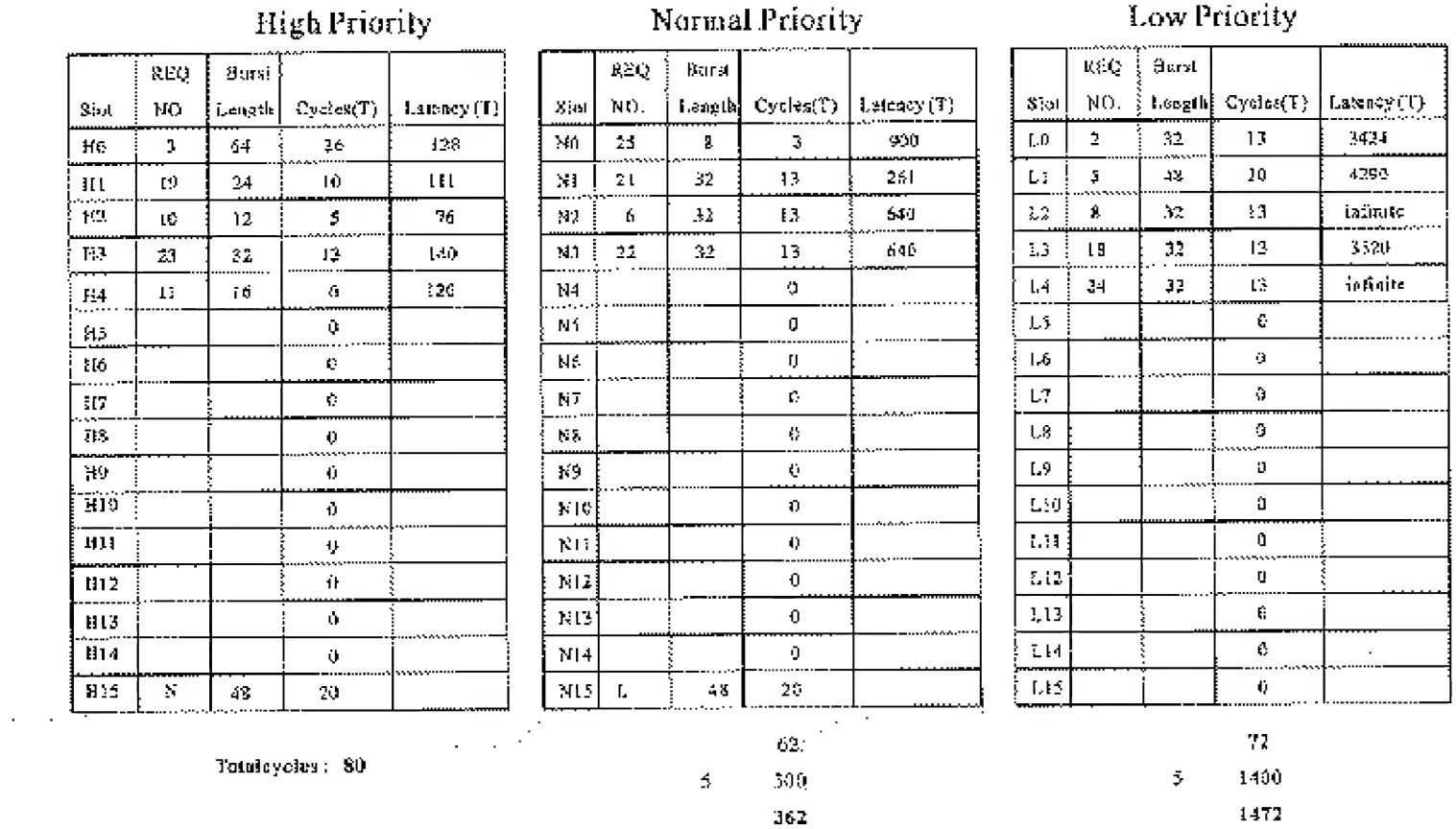

430
OR
707
Next ownership selector unit
704
Ownership MUX
706
Access request MUX
701
Ownership selector
703
Low priority setting register
702

FIG. 7



High Priority

Slot	REQ NO	Burst Length	Cycles(T)	Latency (T)
H0	3	64	36	128
H1	09	24	10	181
H2	16	12	5	96
H3	23	32	12	140
H4	13	16	6	126
H5			0	
H6			0	
H7			0	
H8			0	
H9			0	
H10			0	
H11			0	
H12			0	
H13			0	
H14			0	
H15	N	48	20	

Normal Priority

Slot	REQ NO.	Burst Length	Cycles(T)	Latency (T)
N0	25	8	3	900
N1	21	32	13	261
N2	6	32	13	640
N3	22	32	13	646
N4			0	
N5			0	
N6			0	
N7			0	
N8			0	
N9			0	
N10			0	
N11			0	
N12			0	
N13			0	
N14			0	
N15	L	48	20	

Low Priority

Slot	REQ NO.	Burst Length	Cycles(T)	Latency (T)
L0	2	32	13	3424
L1	5	48	20	4280
L2	8	32	13	infinite
L3	18	32	13	3520
L4	34	32	13	infinite
L5			0	
L6			0	
L7			0	
L8			0	
L9			0	
L10			0	
L11			0	
L12			0	
L13			0	
L14			0	
L15			0	

Totalcycles : 80

62:

5 300

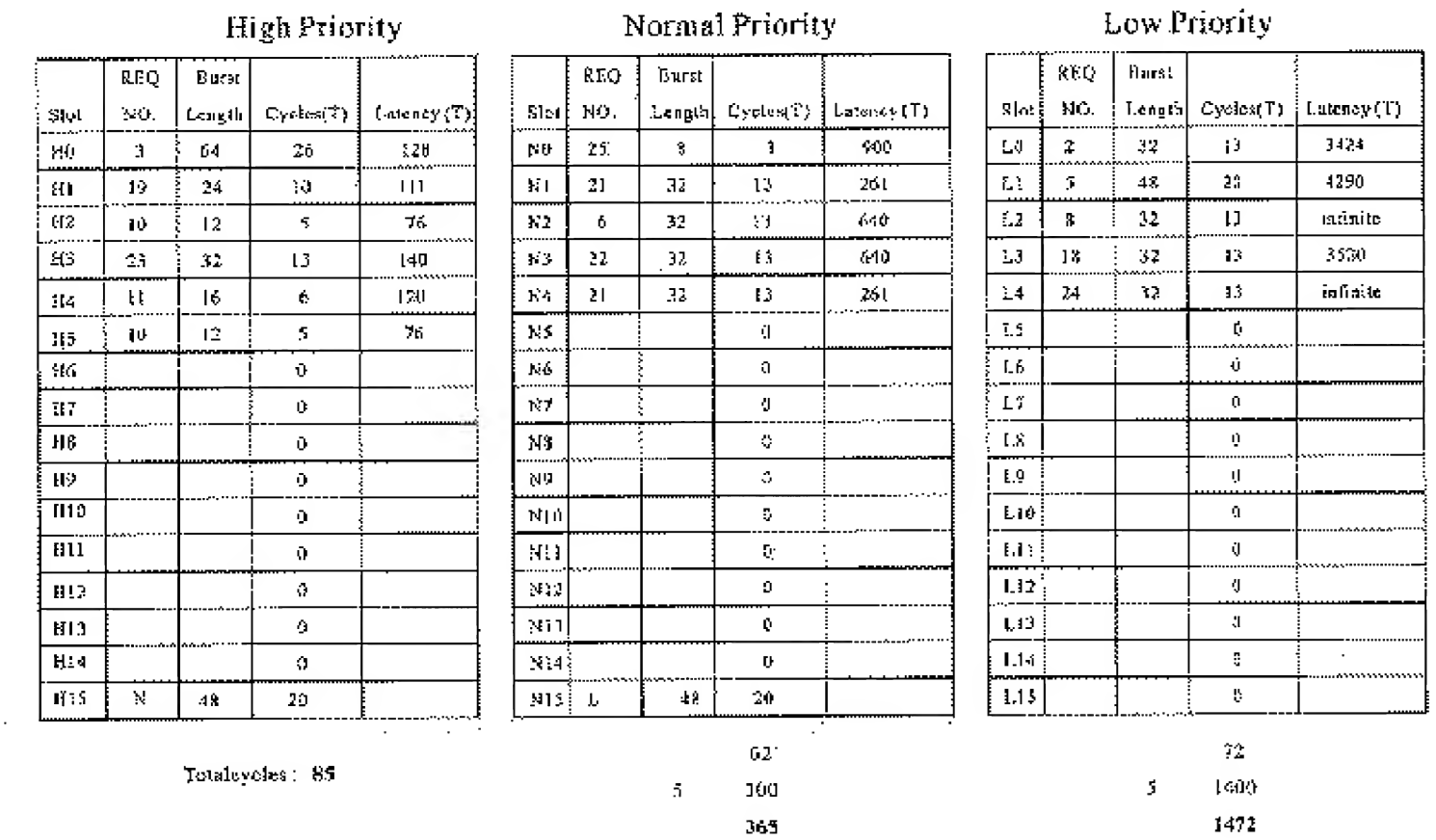
362

72

5 1400

1472

FIG. 8



High Priority

Slot	REQ NO.	Burst Length	Cycles(T)	Latency(T)
H0	3	64	26	328
H1	19	24	10	111
H2	10	12	5	76
H3	25	32	13	140
H4	11	16	6	120
H5	10	12	5	76
H6			0	
H7			0	
H8			0	
H9			0	
H10			0	
H11			0	
H12			0	
H13			0	
H14			0	
H15	N	48	20	

Totalcycles : 85

Normal Priority

Slot	REQ NO.	Burst Length	Cycles(T)	Latency(T)
N0	25	8	3	900
N1	21	32	13	261
N2	6	32	13	640
N3	22	32	13	640
N4	21	32	13	261
N5			0	
N6			0	
N7			0	
N8			0	
N9			0	
N10			0	
N11			0	
N12			0	
N13			0	
N14			0	
N15	L	48	20	

62

5 300

365

Low Priority

Slot	REQ NO.	Burst Length	Cycles(T)	Latency(T)
L0	2	32	13	3424
L1	5	48	20	4290
L2	8	32	13	infinite
L3	18	32	13	3530
L4	24	32	13	infinite
L5			0	
L6			0	
L7			0	
L8			0	
L9			0	
L10			0	
L11			0	
L12			0	
L13			0	
L14			0	
L15			0	

72

5 1600

1472

FIG. 9